**ECE 429 Lab 6**

**Carry-Ripple Addition I**

**David Cho**

**A20384999**

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**Introduction**

The objective of this lab is to design and create a schematic of a Full Adder, which will be used in the next two labs. A test circuit will be utilized to test the results, which will be further verified by using equivalence checking a full adder implemented in Verilog.

**Theory/Pre-Lab**

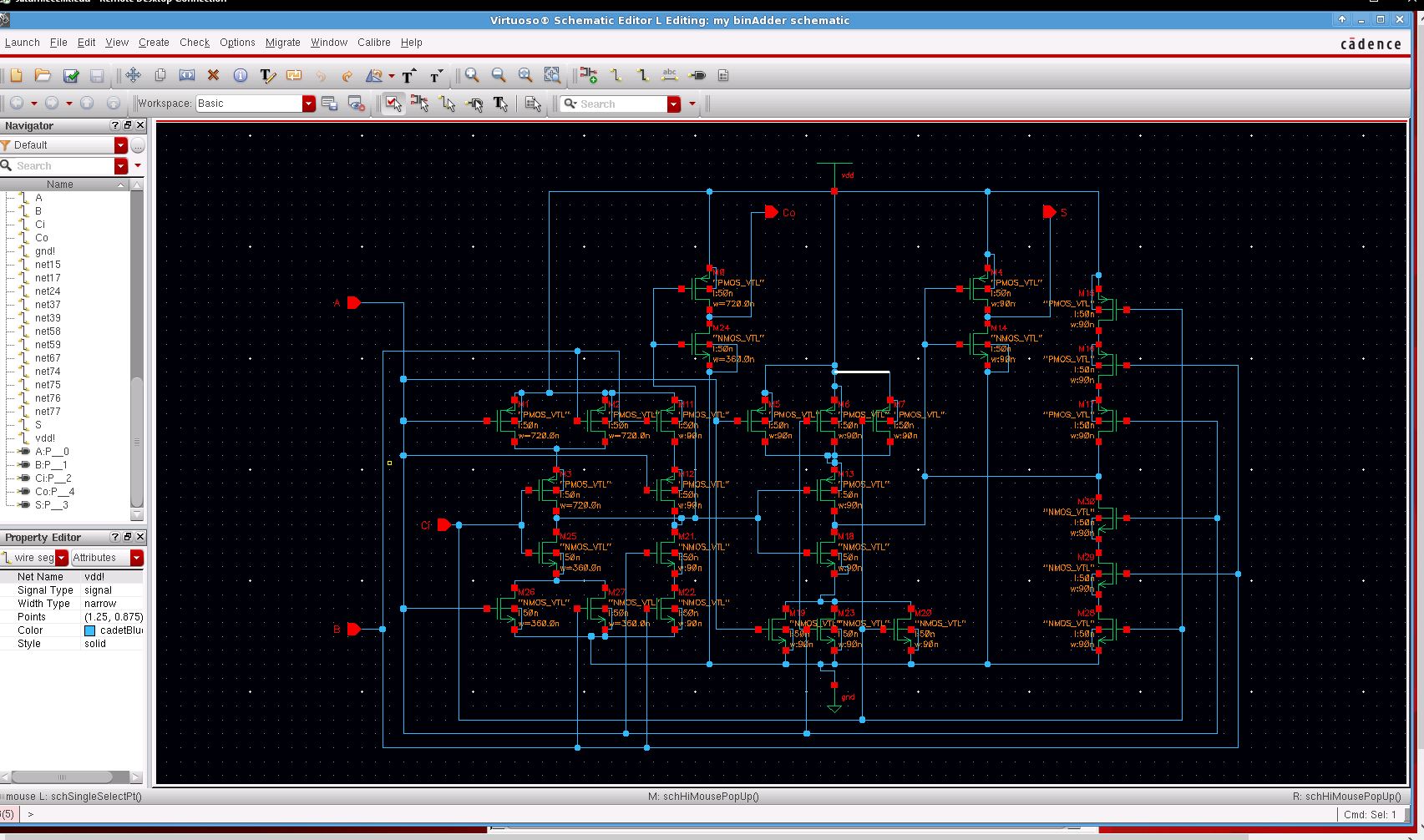
When adding two binary numbers, the addition is done bit-by-bit. Assuming inputs A and B, the sum would be a bit depicted as S. If both A and B were 1, the carryout, C, would be 1, which would then be used in the next bits’ addition. Th full equations can be observed in the lab manual. Several different designs have been proposed, but this lab will utilize the design that reduces the number of transistors required while also increasing the speed of the operation. The mirror adder exploits the following equations of S and C to construct pull-up and pull-down networks that are symmetrical.

Prior to the lab, the mirror adder schematic was observed and tested.

**Implementation**

Using the schematic of the Mirror Adder from the lab manual, the schematic was drawn in Virtuoso

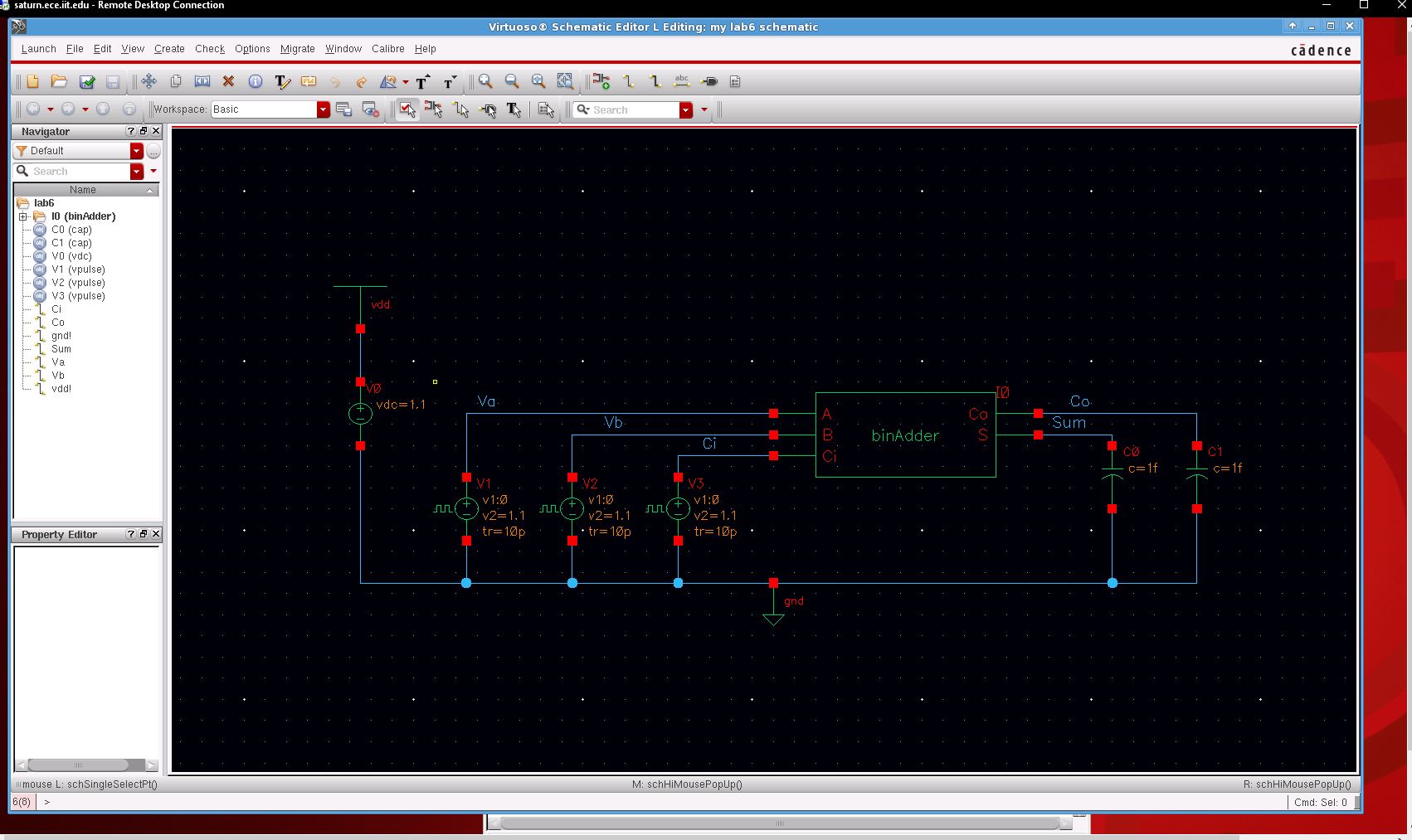
**Figure 1: Schematic of Full-Adder**

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Where the PMOS were indicated as 8 on the given schematic, a width of 720nm was used. Where the NMOS were indicated as 4 on the given schematic, a width of 360nm was used.

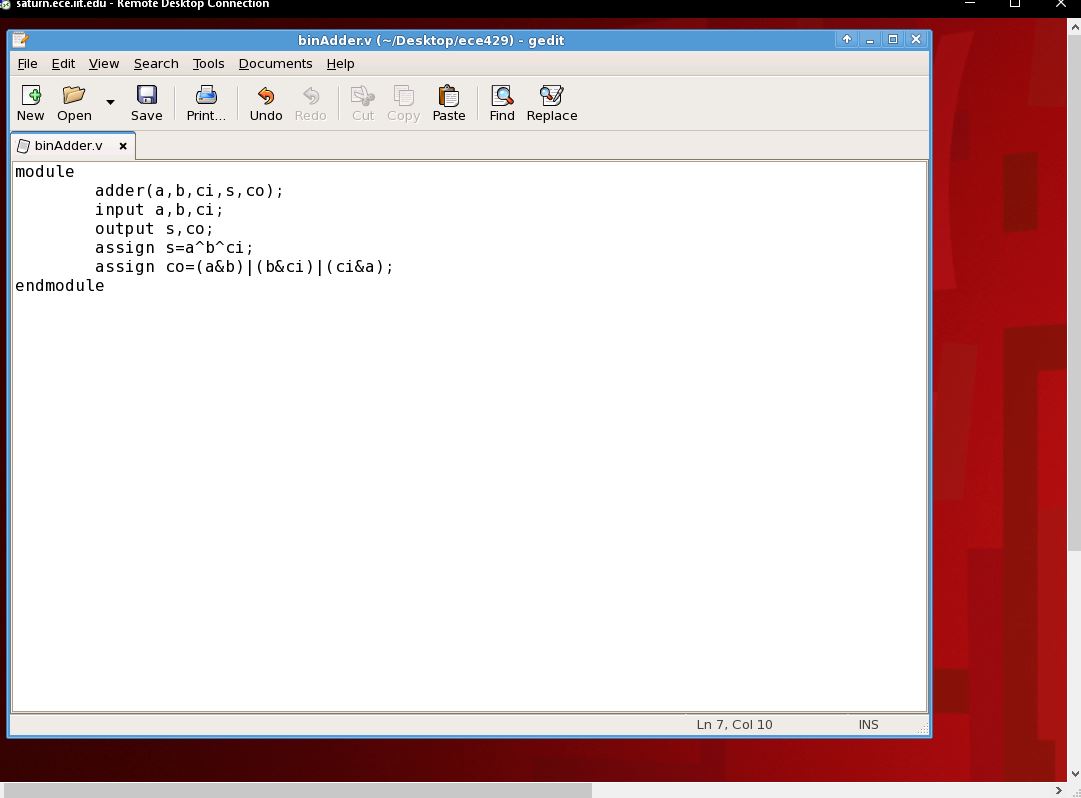
After converting the schematic to a Symbol, a testing circuit was created.

**Figure 2: Test Circuit**

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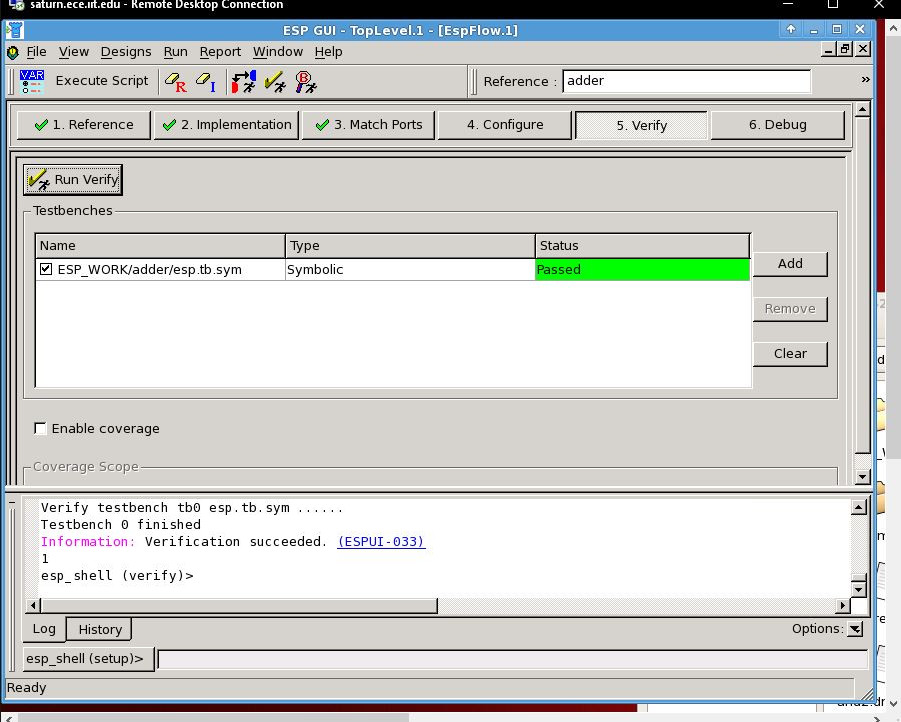
A netlist was generated. For Equivalence checking with ESP, a Verilog file was created.

**Figure 3: Adder Verilog**

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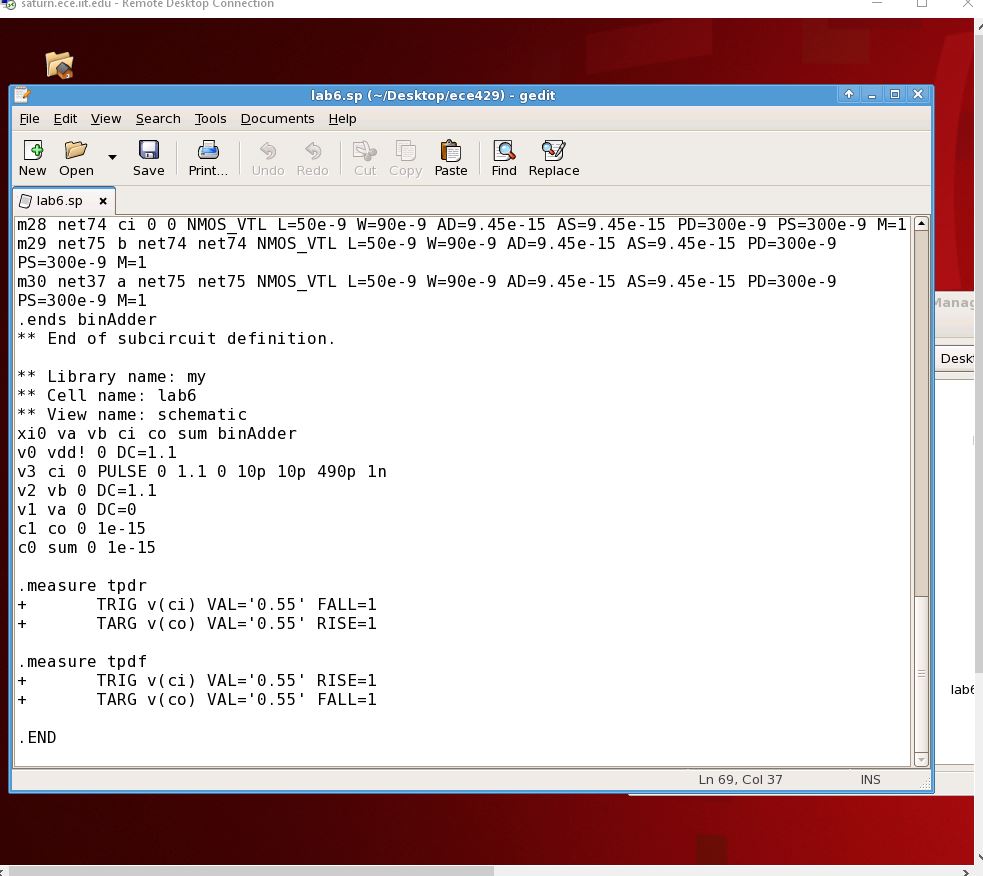
From the generated netlist from the test circuit, Formality ESP was used to verify the circuit.

**Figure 4: Formality Pass**

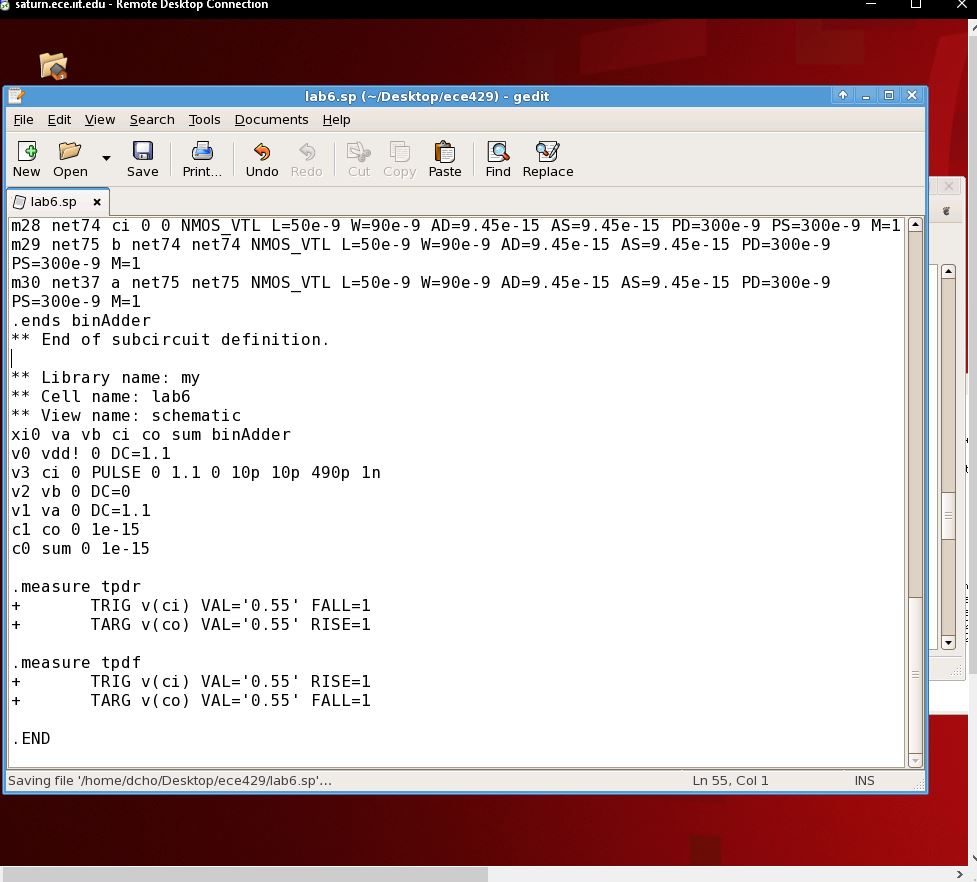
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The netlist was then modified to test different transitions.

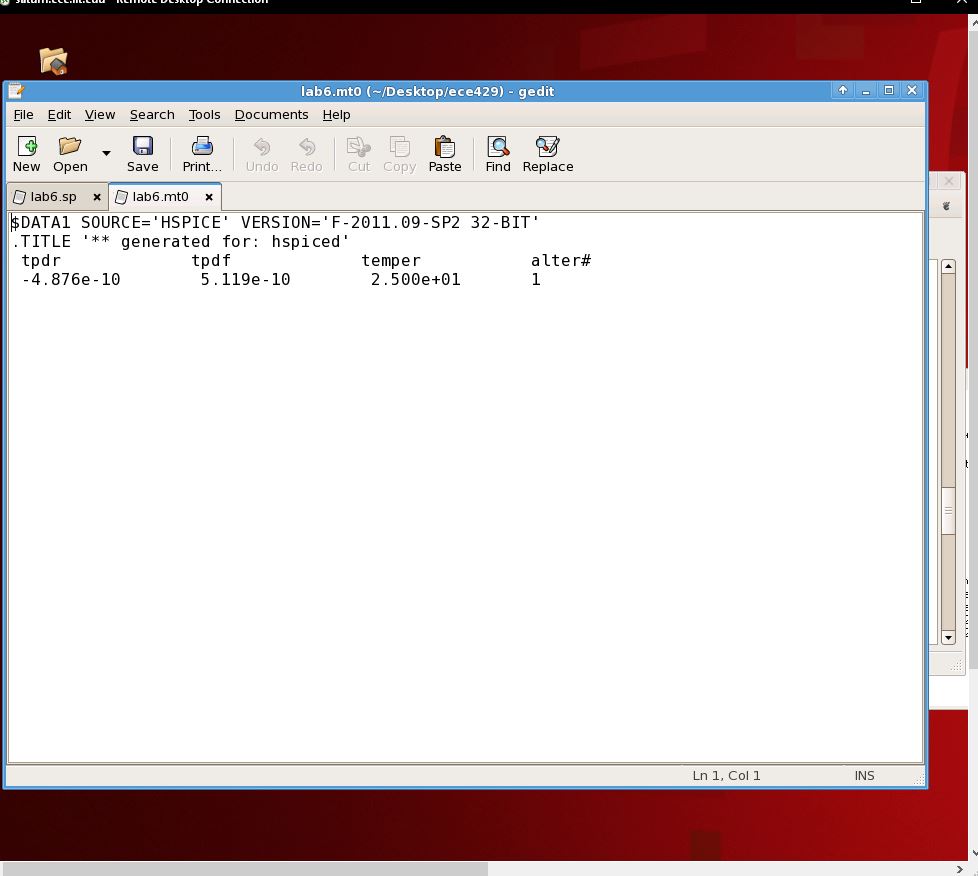
**Figure 5: A, B, Ci 010🡪011 Modified Netlist**

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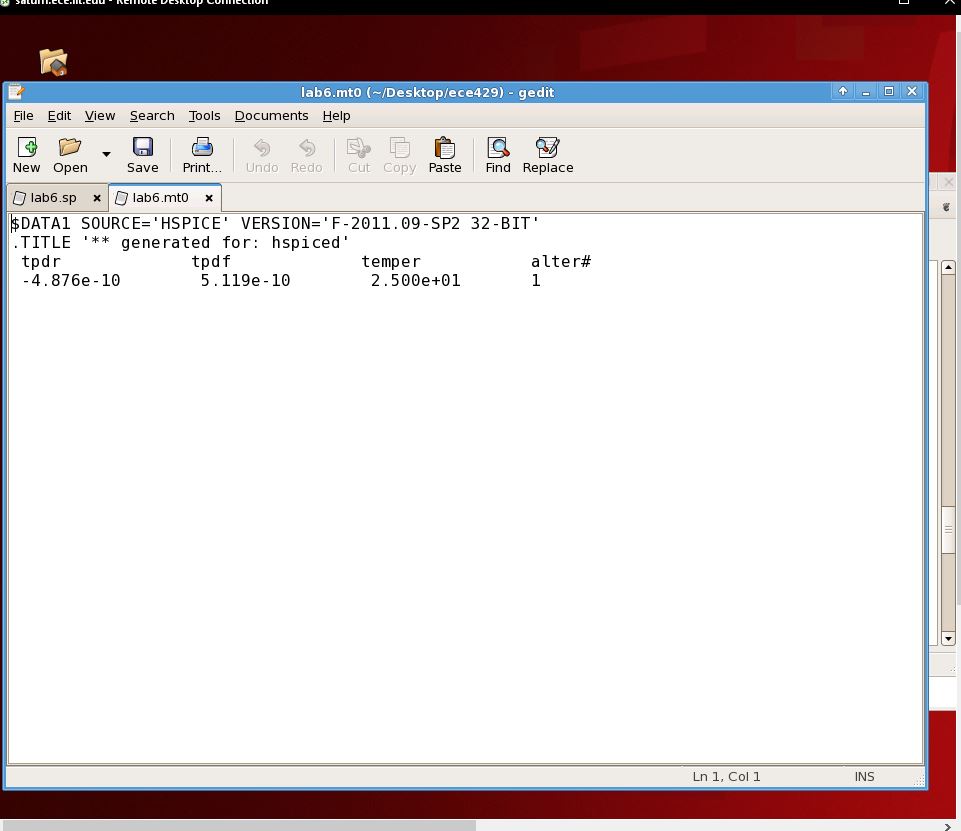
**Figure 6: A, B, Ci 100🡪101 Modified Netlist**

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The Netlists were simulated with HSpice to measure the tpdr and tpdf.

**Figure 7: A, B, Ci 010🡪011 Measurement**

**Figure 8: A, B, Ci 100🡪101 Measurement**

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**Deliverable Questions**

1. The transistors are sized differently in order to minimize delay. The standard ratio for delay optimization is 2:1 PMOS width to NMOS width. ci is used the inner inputs in order to optimize the reduction in delay.

**Conclusion**

In conclusion, this was a successful lab. The schematic for the full adder was successfully implemented and verified. The measured results were as expected, and the Verilog equivalence check was passed.